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From: Edward B. Weller
Reg No. 37,468
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Client-Matter Number: 2102487-991320

Re: U.S. Patent Application No. 10/762,156

Pages: - 6 - (including this form) Originals: ☐ will be mailed ☒ will not be mailed

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Message:

Transmitted via Fax on: June 17, 2005
Attorney Docket No. 2102487-991320
U.S. Patent Application No. 10/762,156
Filing Date: January 20, 2004
Title: SEMICONDUCTOR INTEGRATED CIRCUIT HAVING AN OBLIQUE GLOBAL SIGNAL
WIRING AND SEMICONDUCTOR INTEGRATED CIRCUIT WIRING METHOD

Enclosed is:

1. Response to Restriction Requirement

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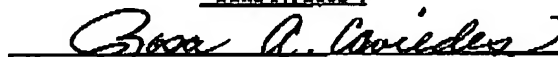
App. Serial No. : 10/762,156
Applicant : Naohito Kojima
Filed : January 20, 2004
Art Unit : 2811
Examiner : Loke, Stevan Ho Yin

Atty. Docket No. : 2102487-991320
Customer No. : 26379

Title: **SEMICONDUCTOR INTEGRATED CIRCUIT HAVING AN OBLIQUE
GLOBAL SIGNAL WIRING AND SEMICONDUCTOR INTEGRATED
CIRCUIT WIRING METHOD**

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RESPONSE TO RESTRICTION REQUIREMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the restriction requirement mailed on May 19, 2005, Applicant hereby elects to prosecute species 1, Figs. 2-16, with corresponding claims 1-6, 8, 12-13 without traversal.

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 5 of this paper.

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